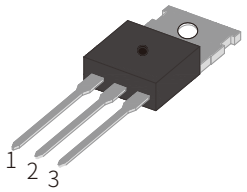
FEATURES

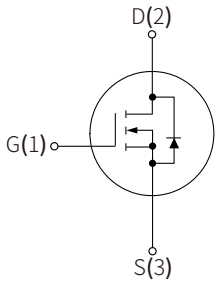
- Advanced trench cell design
- Low Thermal Resistance
- Super Trench



TO-220C

APPLICATIONS

- Motor drivers
- DC - DC Converte



Schematic Symbol

APPROVALS

RoHS	Compliance with 2011/65/EU
HF	Compliance with IEC61249-2-21:2003

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-source voltage	V_{DSS}	T_j= 25 °C to 150°C			500	V
Drain-gate voltage	V_{DGR}	T_j= 25 °C to 150°C;R_{GS} = 20 kΩ			500	V
Gate-source voltage	V_{GS}				±30	V
Continuous drain current	I_D	T_{mb} = 25 °C; V_{GS} = 10 V			8.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V			5.4	
Pulsed drain current	I_{DM}	T_{mb} = 25 °C			34	A
Total dissipation	P_D	T_{mb} = 25 °C			147	W
Operating junction and storage temperature range	T_j, T_{stg}		-55		150	°C
Non-repetitive avalanche energy	E_{AS}	Unclamped inductive load, I_{AS} = 7.4 A;t_p = 0.22 ms; T_j prior to avalanche = 25°C;V_{DD} ⩽ 50 V; R_{GS} = 50 Ω; V_{GS} = 10 V; refer to fig:17			531	mJ
Repetitive avalanche energy (Notes1)	E_{AR}	I_{AR} = 8.5 A; t_p = 2.5 μs; T_j prior to avalanche = 25°C;R_{GS} = 50 Ω; V_{GS} = 10 V;refer to fig:18			13	mJ
Repetitive and non-repetitive avalanche current	I_{AS}, I_{AR}				8.5	A
Thermal resistance junction	$R_{th\ j\text{-}mb}$	in free air			0.85	K/W
Thermal resistance junction	$R_{th\ j\text{-}a}$	in free air		60		K/W

Notes: (1) pulse width and repetition rate limited by $T_j$max.

ELECTRICAL CHARACTERISTICS(T_A=25°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=0.25mA	500			V
Drain-source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$	V_{DS}=V_{GS},I_D=0.25mA		0.1		%/K
Drain-source On Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=4.8A		0.6	0.85	Ω
Gate Threshold Voltage	$V_{GS(To)}$	V_{DS}=V_{GS},I_D=0.25mA	2	3	4	V
Forward Transconductance	g_{fs}	V_{DS}=30V,I_D=4.8A	3.5	6		S
Drain-source Leakage Current	I_{DSS}	V_{DS}=500V,V_{GS}=0V		1	25	μA
		V_{DS}=400V,V_{GS}=0V,T_j= 125 °C		40	250	
Gate-source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V		10	200	nA
Total Gate Charge	$Q_{Qg(tot)}$	I_D = 8.5 A; V_{DD} = 400 V; V_{GS} = 10 V		55	80	nC
Gate Source Charge	Q_{gs}			5.5	7	
Gate-drain (Miller) Charge	Q_{gd}			30	45	
Turn–on Delay Time	$t_{d(on)}$	V_{DD} = 250 V; R_D = 30 Ω; R_G = 9.1 Ω		18		ns
Turn–on Rise Time	t_r			37		
Turn–off Delay Time	$t_{d(off)}$			80		
Turn–off Fall Time	t_f			36		
Internal Drain Inductance	L_d	Measured from tab to centre of die		3.5		nH
Internal Drain Inductance	L_d	Measured from drain lead to centre of die		4.5		
Internal Source Inductance	L_s	Measured from source lead to source bond pad		7.5		
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V, f =1MHz		960		pF
Output Capacitance	C_{oss}			140		
Feedback Capacitance	C_{rss}			80		
Source-drain Diode Ratings And Characteristics						
Continuous Source Current (Body Diode)	I_S	T_{mb} = 25°C			8.5	A
Pulsed Source Current (Body Diode)	I_{SM}	T_{mb} = 25°C			34	A
Diode Forward Voltage	V_{SD}	I_S = 8.5 A; V_{GS} = 0 V			1.2	V
Reverse Recovery Time	t_{rr}	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/μs		440		ns
Reverse Recovery Charge	Q_{rr}			6.4		μC

PARAMETER CHARACTERISTIC CURVE

Figure 1: Normalised power dissipation.
$PD\% = 100.P_D/P_{D25\,°C} = f(T_{mb})$

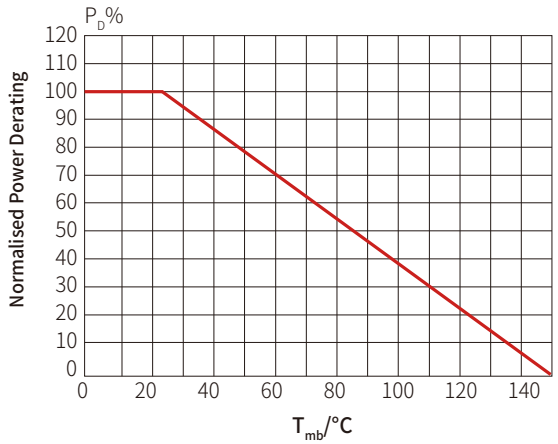


Figure 2: Normalised continuous drain current.
$ID\% = 100.ID/I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geqslant 10$ V

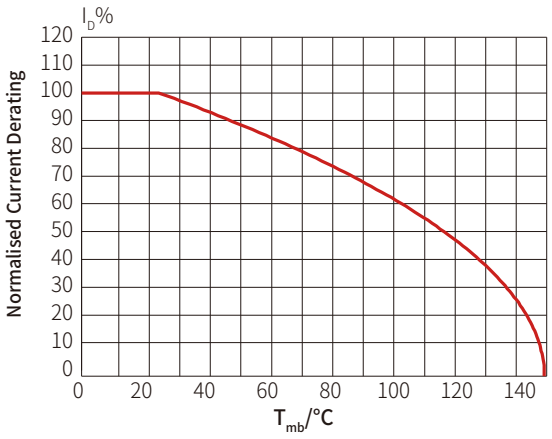


Figure 3: Safe operating area. $T_{mb} = 25°C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

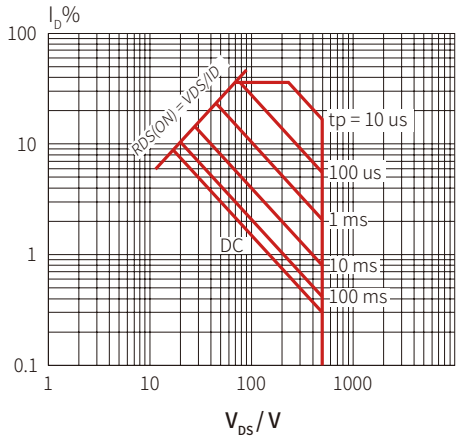


Figure 4: Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

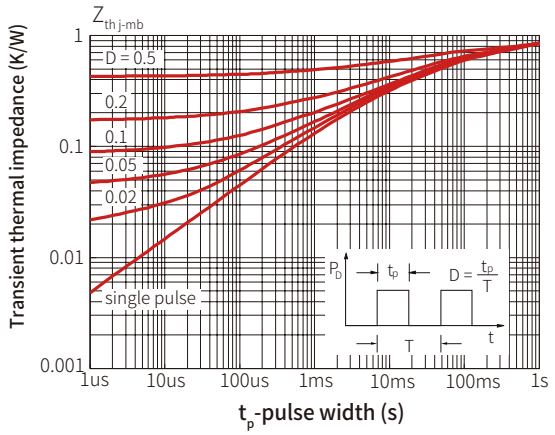


Figure 5: Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

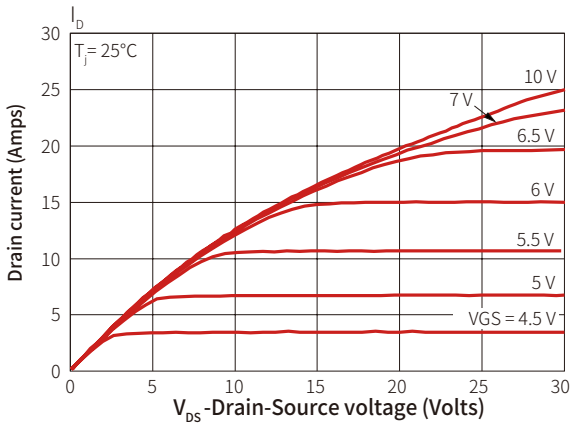


Figure 6: Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

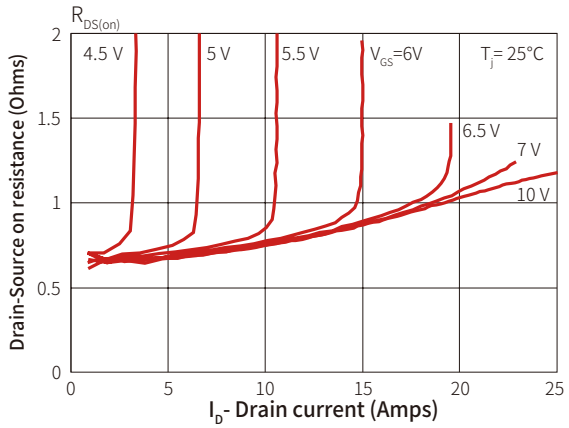


Figure 7: Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

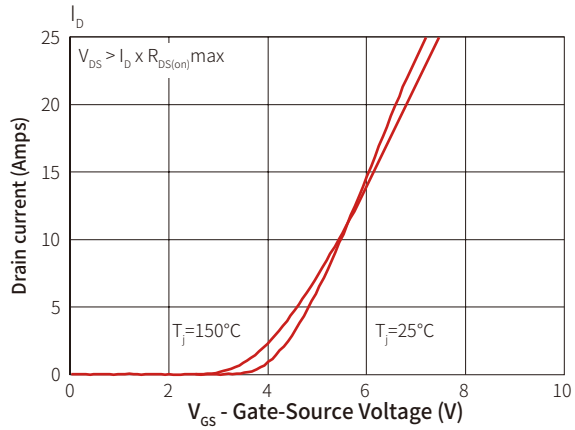


Figure 8: Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

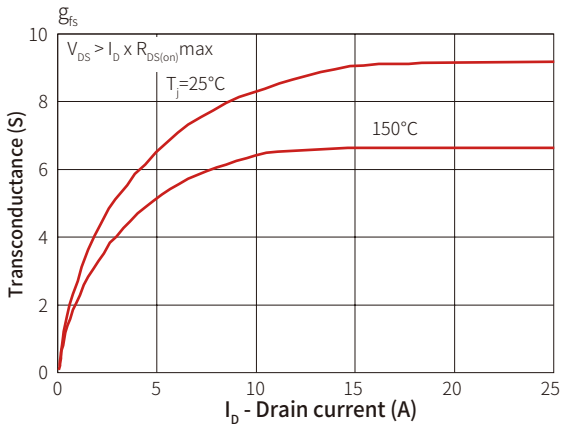


Figure 9: Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D= 4.25 A; V_{GS} = 10 V

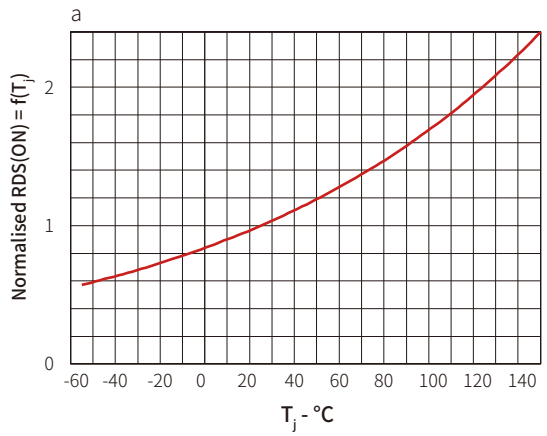


Figure 10: Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

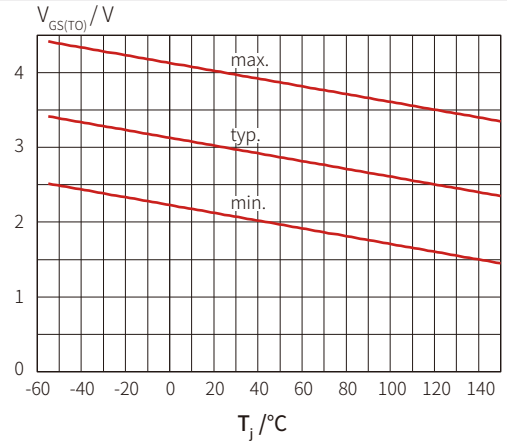


Figure 11: Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j= 25°C; $V_{DS} = V_{GS}$

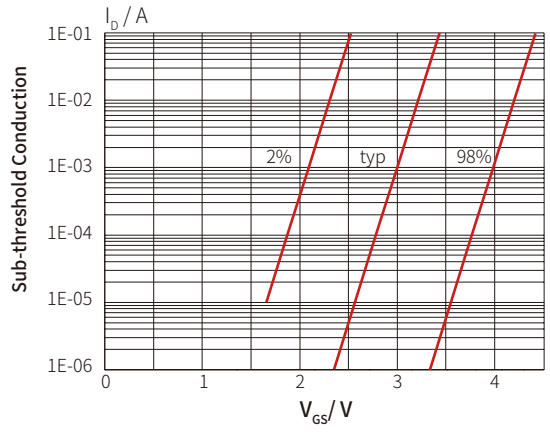


Figure 12: Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f =1MHz

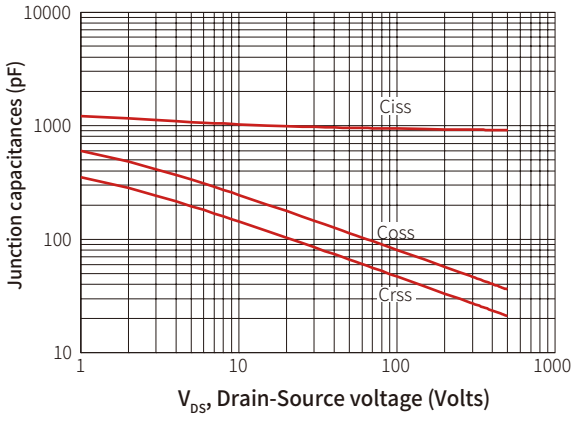


Figure 13: Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

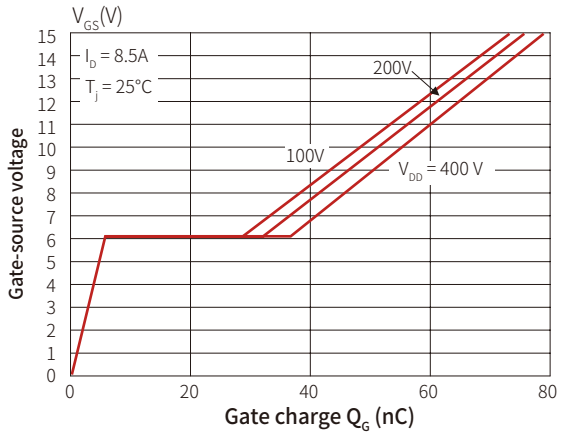


Figure 14: Typical switching times; $t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

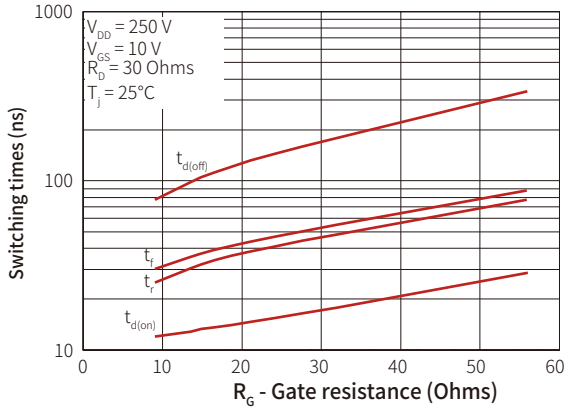


Figure 15: Normalised drain-source breakdown voltage; $V_{(BR)DSS}/V_{(BR)DSS\ 25\,°C} = f(T_j)$

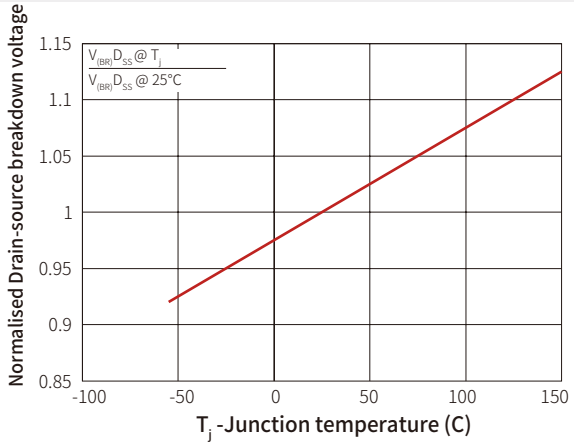


Figure 16: Source-Drain diode characteristic. $I_F = f(V_{SDS})$; parameter T_j

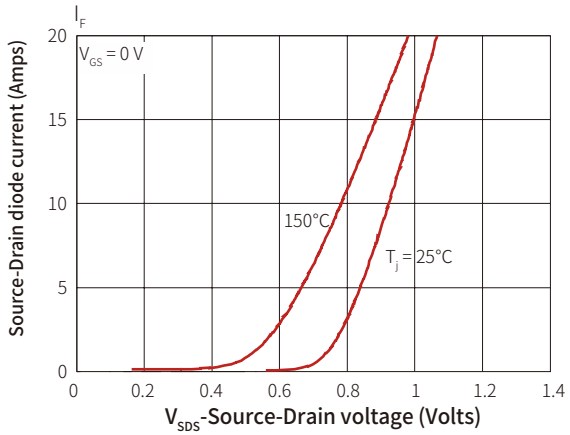


Figure 17: Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

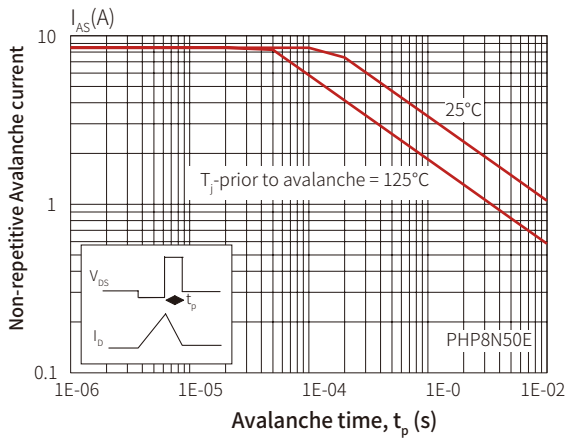
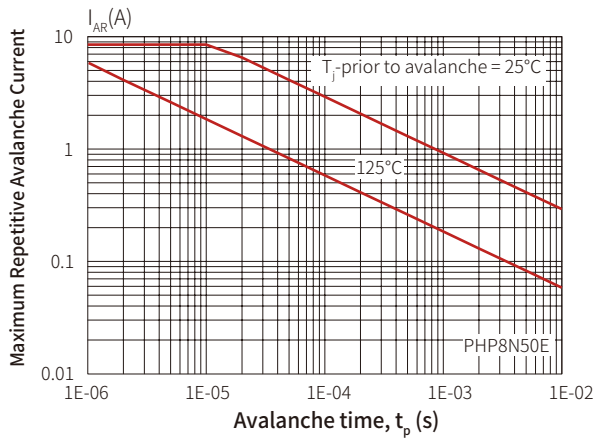
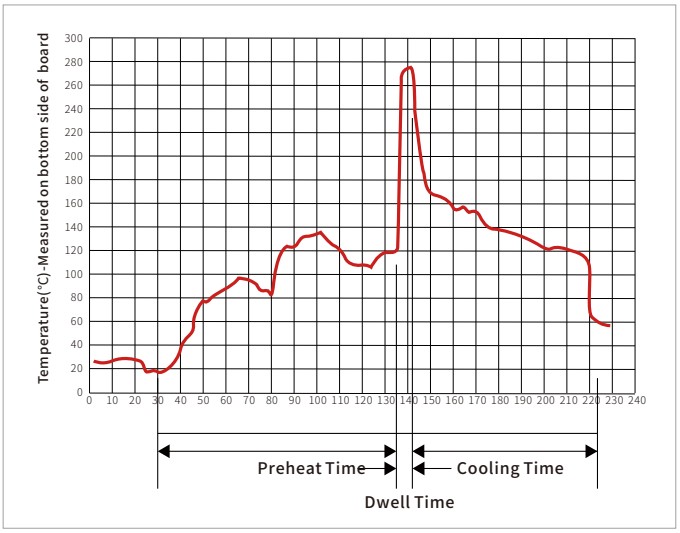


Figure 18: Maximum permissible repetitive avalanche current (I_{AR}) versus avalanche time (t_p)

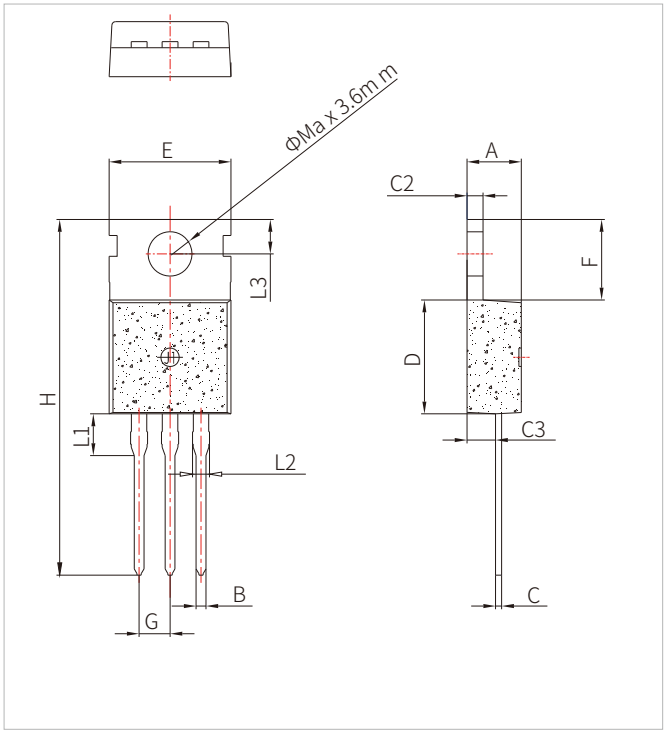


WAVE SOLDERING



Wave Parameter		Lead–free assembly
Pre Heat	Temperature Min	100°C
	Temperature Max	150°C
	Time(min to max)	60 – 180 secs
Solder pot Temperature		280°C Max
Solder Dwell Time		2-5 seconds

TO-220C PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.70	0.169		0.185
B	0.70		0.90	0.028		0.035
C	0.45		0.60	0.018		0.024
C2	1.23		1.32	0.048		0.052
C3	2.20		2.60	0.087		0.102
D	8.80		10.0	0.346		0.394
E	9.90		10.3	0.390		0.406
F	6.30		6.90	0.248		0.272
G		2.54			0.1	
H	28.0		30.0	1.102		1.181
L1		3.10			0.122	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
Φ		3.6			0.142	

ORDERING INFORMATION

Part Number	Package	Qty/pcs		
		Tube	Inner Box	Carton
IRF840	TO-220C	50	1000	5000

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